

**A MEMORY SYSTEM AND METHOD OF ACCESSING THEREOF**

5

Field of the Invention

The present invention relates generally to memory systems and systems utilizing memory systems, and more particularly to systems and methods for accessing information stored in memory systems.

10

Related Art

Data is stored in a nonvolatile memory as charge on floating gate electrodes of field-effect transistors (FETs), which in turn make up the memory cells of the nonvolatile memory.

When measuring charge on the floating gate electrode (i.e., reading data from the memory cell), an electric field appears across the tunnel oxide located between the floating gate electrode and the channel region of the FET of the memory cell. This electric field can cause charge stored on the floating gate electrode to leak off. The electric field seen by the floating gate electrode is smaller during read operations than during write operations, but a nonvolatile memory may be read continuously for a large part of its life. After such

20 prolonged periods of exposure to an electric field, the charge stored on the floating gate electrode can change, and cause a low threshold state to be indistinguishable from a high threshold state during a read operation. This results in a “read disturb” of the memory cell.

FIG. 1 illustrates a conventional memory system 100. The memory system 100 has a nonvolatile memory array 110; a column decoder 120 coupled to the memory array 110 via column lines CL1, CL2, CL3 and CL4; and a row decoder 130 coupled to the memory array 110 via row lines RL1, RL2, RL3 and RL4. The memory array 110 is made up of sixteen memory cells 112 arranged in rows and columns, and numerically designated “1” to “16.” Each of the memory cells 112 has an associated address. Address signals A0, A1, A2 and A3 drive the column and row decoders 120 and 130 to access the memory cells 112 by their 30 associated addresses.

To conserve power and reduce access time, the memory system 100 is designed to access memory cells 112 during read operations along rows in the direction of arrow 140, as illustrated in FIG. 1 with respect to the row associated with row line RL1, and in the order of

the numerical designations "1" to "16." The address signals A0, A1, A2 and A3 are formatted such that consecutive memory cell addresses are associated with memory cells arranged along the same row of the memory array 110. Unfortunately, such accessing subjects the memory system 100 to read disturb. Read disturb, as mentioned earlier, occurs 5 when the net charge on a memory cell's floating gate changes over time due to the bias voltage which is applied during read operations. If the memory system 100 is accessed to continuously cycle among only some of the memory cells, for example those memory cells 112 designated "1," "2" and "3," then read disturb stress will be focused along the row associated with row line RL1 of the memory array 110.

10 What is needed is a memory system and a method of accessing a memory system that minimizes read disturb.

#### Brief Description of the Drawings

15 The present invention is illustrated by way of example and not limitation in the accompanying figures, in which:

FIG. 1 is a block diagram illustrating a prior art memory system;

FIG. 2 is a block diagram illustrating a memory system according to an embodiment of the present invention;

20 FIG. 3 is a block diagram illustrating an embedded control system having a memory system according to another embodiment of the present invention;

FIG. 4 is a diagram illustrating information in a page format suitable for use with the memory system of FIG. 2, 3, 5 or 6;

25 FIG. 5 is a block diagram of an embedded control system having a memory system according to yet another embodiment of the present invention;

FIG. 6 is a block diagram of an embedded control system having a memory system according to yet another embodiment of the present invention;

FIG. 7 is a diagram illustrating an addressing format suitable for use in the memory system of FIG. 2, 3, 5 or 6;

30 FIG. 8 is a schematic diagram illustrating a portion of a memory array suitable for use in the memory system of FIG. 2, 3, 5 or 6; and

FIG. 9 is a diagram illustrating a prior art addressing format.

Detailed Description

5 A memory system has an array of addressable storage elements arranged in a plurality of rows and a plurality of columns, and decoding circuitry coupled to the array of addressable storage elements. The decoding circuitry, in response to decoding a first address, accesses a first storage element of a first row of the plurality of rows, and, in response to decoding a second address consecutive to the first address, accesses a second storage element of a second 10 row of the plurality of rows. The second row of the plurality of rows is different from the first row of the plurality of rows. By implementing a memory system wherein consecutive addresses correspond to storage elements of different rows, read disturb stresses along a single row can be minimized.

15 FIG. 2 illustrates a memory system 200. The memory system 200 has a memory array 210, and decoding circuitry 220 and 230 coupled to the memory array 210. The memory array 210 is an array of addressable storage elements 212 arranged in a plurality of rows and a plurality of columns. The storage elements 212 may be any suitable memory including but not limited to RAM (random access memory), ROM (read-only memory), EEPROM (electrically erasable programmable read-only memory), and the like. In the embodiment 20 illustrated in FIG. 2, the memory array 210 has sixteen addressable storage elements numerically designated "1" to "16." The addressable storage elements 212 are operable to store data such as an individual bit of digital information; a plurality of bits arranged as a byte, a word or a page; or any other convenient unit of information storage. The decoding circuitry 220 and 230 is made up of a column decoder 220 coupled to the memory array 210 via column lines CL1, CL2, CL3 and CL4 and a row decoder 230 coupled to the memory array 210 via row lines RL1, RL2, RL3 and RL4. The column and row decoders 220 and 230 operate responsive to address signals A0, A1, A2 and A3 to access the addressable storage elements 212 during read operations.

25 Unlike the conventional memory system 100 of FIG. 1, the memory system 200 of FIG. 2 accesses memory cells 212 along columns in the direction of arrow 240, as illustrated in FIG. 2 with respect to the column associated with column line CL1, and in the order of the

memory cells' 212 numerical designations 1 to 16. The address signals A0, A1, A2 and A3 are formatted such that consecutive memory cell addresses are associated with memory cells arranged along different rows of the memory array 210. This accessing of the memory array 210 reduces the probability that a single row line will be continuously activated during a read 5 operation and, thereby, reduces read disturb. For example, when accessing memory cells 212 designated 1 to 4, row lines RL1 to RL4 are used, thereby distributing read disturb stress across the entire memory array 210 rather than focusing read disturb stress along a single row of the memory array 210. Other arrangements that spread read disturb stress across multiple rows are shown in FIGs. 3, 5 and 6.

10 FIG. 3 illustrates an embedded control system 300 having a processor 302 and a memory system 301 coupled to the processor 302. The memory system 301 has an input to receive an address signal, shown as row and column address signals  $A_0 \dots A_M$  and  $A_M \dots (A_{M+N})$ , from the processor 302, and an output to send addressed information in the form of a data signal DATA [0:Z] to the processor 302. The memory system 301 includes decoding 15 circuitry, shown as column decoders 320 and 321 and row decoder 330, and memory arrays 310 and 311. The row decoder 330 is coupled to the memory array 310 via row lines R1, R2, R3 and R4 and to the memory array 311 via row lines R5, R6, R7 and R8. The column decoder 320 is coupled to the memory array 310 via column lines CL1, CL2, CL3, CL4, CL5, CL6, CL7 and CL8. The column decoder 321 is coupled to the memory array 311 via column lines CL1, CL2, CL3, CL4, CL5, CL6, CL7 and CL8. The memory array 310 has 20 memory cells 312 arranged in a plurality of rows and a plurality of columns. The memory array 311 has memory cells 313 arranged in a plurality of rows and a plurality of columns. The memory cells 312 and 313 may be any suitable memory including but not limited to RAM (random access memory), ROM (read-only memory), EEPROM (electrically erasable 25 programmable read-only memory), and the like. The portion of the row decoder 330 driving the memory array 310, the column decoder 320 and the memory array 310 may be collectively referred to as a first memory block BLK1. The portion of the row decoder 330 driving the memory array 311, the column decoder 321 and the memory array 311 may be collectively referred to as a second memory block BLK2. The processor 302 is coupled to 30 the input and output of the memory system 301 via connections 342, 344 and 346. The processor 302 sends the row address signal  $A_0 \dots A_M$  to the row decoder 330 via the

connection 342; sends the column address signal  $A_M \dots (A_{M+N})$  to the column decoders 320 and 321 via connection 344; and receives addressed information as the data signal DATA [0:Z] from the column decoders 320 and 321 via connection 346.

The memory system 301 of FIG. 3 is a page memory system. The memory cells 312 of the memory array 310 are designated P1 to P32. The memory cells 313 of the memory array 311 are designated P33 to P64. The "P" prefix of the designations indicates that each of the memory cells 312 and 313 is operable to store a page of information (or simply "page"), such as in the format illustrated in FIG. 4. Page P of FIG. 4 is made up of eight words W1, W2, ..., W7 and W8. Each of the words W1, W2, ..., W7 and W8 is made up of 32 bits. It will be appreciated depending on the intended use of the memory system 301, page P may contain more or less than eight words and each word may contain more or less than 32 bits.

Referring back to FIG. 3, the numerical suffixes "1" to "64" used in the designations of the memory cells 312 and 313 generally describe the order in which the processor 302 accesses the memory cells 312 and 313 during a read operation. In general, the decoding circuitry 320, 321 and 330 accesses a first page of a first row of the memory array 310 or 311 in response to an address signal having a first address, accesses a second page of a second row of the memory array 310 or 311 in response to the address signal having a second address consecutive to the first address and outputs the first and second pages. In particular, the processor 302 formats the address signals  $A_0 \dots A_M$  and  $A_M \dots (A_{M+N})$  to contain consecutive addresses associated with memory cells arranged along different rows of the memory arrays 310 and 311. The row decoder 330 upon receiving and decoding the address signals  $A_0 \dots A_M$  would activate row line RL1 to access memory cells P1, P3, P5, P7, P9, P11, P13 and P15; would activate row line RL2 to access memory cells P2, P4, P6, P8, P10, P12, P14 and P16; would activate row line RL3 to access memory cells P17, P19, P21, P23, P25, P27, P29 and P31; would activate row line RL4 to access memory cells P18, P20, P22, P24, P26, P28, P30 and P32; would activate row line RL5 to access memory cells P33, P35, P37, P39, P41, P43, P45 and P47; would activate row line RL6 to access memory cells P34, P36, P38, P40, P42, P44, P46 and P48; would activate row line RL7 to access memory cells P49, P51, P53, P55, P57, P59, P61 and P63; and would activate row line RL8 to access memory cells P50, P52, P54, P56, P58, P60, P62 and P64. The column decoders 320 and 321, upon receiving and decoding the address signals  $A_M \dots (A_{M+N})$ , would operate in

association with the row decoder 330 by activating respective column lines CL1 to CL8 accordingly. Pages from the accessed memory cells are output in the form of the data signal DATA [0:Z]. Therefore, in a common data read or write scenario in which pages must be cyclically and sequentially read from or written to only a small number of memory cells of 5 the memory system 301, such as the memory cells designated P1, P2, P3, P4, P5, P6, P7 and P8, the embedded control system 300 would effectively distribute read disturb stress across two different rows of the memory array 310.

FIG. 7 illustrates an addressing format 700 used by the processors 302 to create the address signals  $A_0 \dots A_M$  and  $A_M \dots (A_{M+N})$  and, for purposes of clarity, is discussed in 10 conjunction with a conventional addressing format 900 shown in FIG. 9. The conventional addressing format 900 of FIG. 9 shows address bits arranged from least significant bit LSB to most significant bit MSB, wherein less significant address bits A0 to A10 are used to address columns 902 of a memory array, and more significant bits A11 to An are used to address rows 904 of a memory array. The addressing format 700 of FIG. 7 shows numeric address 15 bits arranged from least significant bit LSB to most significant bit MSB; however, unlike the conventional addressing format 900 of FIG. 9, the addressing format 700 of FIG. 7 uses some of the less significant bits A0 to A10 to address rows 704 and 708 of a memory array and some of the more significant bits A11 to An to address columns 702 and 706 of the memory array. Specifically, address bits A0 to A7 are used to address columns 702, address bits A14 20 to A16 are used to address columns 706, address bits A8 to A13 are used to address rows 704, and A17 to An are used to address rows 708. In addressing format 700, least significant bits A0 to A4 are representative of addresses of bits within a word, next least significant bits A5 to A7 are representative of addresses of words within a page, intermediate significant bits A8 to A13 are representative of addresses of rows, more significant bits A14 to A16 are 25 representative of addresses of pages within rows and next more significant bits A17 to An are representative of addresses of memory blocks. By interposing row addressing between column addressing and using less significant bits to address rows, the addressing format 700 prevents large numbers of sequential pages from being accessible via a single row line.

FIG. 5 illustrates a second embedded control system 500 similar in structure to the 30 embedded control system 300 of FIG. 3. The embedded control system 500 of FIG. 5 has a memory system 501 with a row decoder 530, column decoders 520 and 521, memory arrays

510 and 511, memory cells 512 and 513 (and memory blocks BLK1 and BLK2) arranged and interconnected in substantially the same manner as the counterpart structure in FIG. 3. The embedded control system 500 of FIG. 5 has a processor 502 and connections 542, 544 and 546 to carry row address signal  $B_0 \dots B_M$ , column address signal  $B_M \dots (B_{M+N})$  and data 5 signal DATA [0:Y], respectively, arranged and interconnected in substantially the same manner as the counterpart structure in FIG. 3. The memory system 501 is a page memory system with the memory cells 512 and 513 designated P1 to P32 and P33 to P64, respectively, and each of the memory cells 512 and 513 being operable to store a page.

The embedded control system 500 of FIG. 5 departs from the embedded control 10 system 300 of FIG. 3 in the specific manner that the processor 502 formats the address signals  $B_0 \dots B_M$  and  $B_M \dots (B_{M+N})$  to contain consecutive addresses associated with memory cells arranged along different rows of the memory arrays 510 and 511. The row decoder 330 upon receiving and decoding the address signals  $B_0 \dots B_M$  would activate row line RL1 to access memory cells P1, P5, P9, P13, P17, P21, P25 and P29; would activate row 15 line RL2 to access memory cells P2, P6, P10, P14, P18, P22, P26 and P30; would activate row line RL3 to access memory cells P3, P7, P11, P15, P19, P23, P27 and P31; would activate row line RL4 to access memory cells P4, P8, P12, P16, P20, P24, P28 and P32; would activate row line RL5 to access memory cells P33, P37, P41, P45, P49, P53, P57 and P61; would activate row line RL6 to access memory cells P34, P38, P42, P46, P50, P54, P58 20 and P62; would activate row line RL7 to access memory cells P35, P39, P43, P47, P51, P55, P59 and P63; and would activate row line RL8 to access memory cells P36, P40, P44, P48, P52, P56, P60 and P64. The column decoders 520 and 521, upon receiving and decoding the address signals  $B_M \dots (B_{M+N})$ , would operate in association with the row decoder 530 by activating respective column lines CL1 to CL8 accordingly. Pages from the accessed 25 memory cells are output in the form of the data signal DATA [0:Y]. Therefore, in a common data read or write scenario in which pages must be cyclically and sequentially read from or written to only a small number of memory cells of the memory system 501, such as memory cells designated P1, P2, P3, P4, P5, P6, P7 and P8, the embedded control system 500 would effectively distribute read disturb stress across four different rows of the memory array 510.

30 FIG. 6 illustrates a third embedded control system 600. The structure of the embedded control system 600, like the structure of the embedded control system 300 of FIG.

3, has a memory system 601 made up of two memory arrays 610 and 611 with memory cells 612 and 613, respectively, and two column decoders 620 and 621 coupled to respective ones of the memory arrays 610 and 611 by column lines CL1 to CL8. The structure of the embedded control system 600 of FIG. 6, like the structure of the embedded control system 5 300 of FIG. 3, has a processor 602 and connections 642, 644 and 646 to carry row address signal  $C_0 \dots C_M$ , column address signal  $C_M \dots (C_{M+N})$  and data signal DATA [0:X], respectively. Unlike the embedded control system 300 of FIG. 3, the memory system 601 of the embedded control system 600 of FIG. 6 employs two distinct row decoders 630 and 631. The row decoder 630 is coupled to the processor 602 via connection 642 and to the memory 10 array 610 via row lines RL1 to RL4. The row decoder 631 is coupled to the processor 602 via connection 642 and to the memory array 611 via row lines RL5 to RL8. In FIG. 6, a first memory block BLK1 is made up of the row decoder 630, the column decoder 620 and the memory array 610; and a second memory block BLK2 is made up of the row decoder 631, the column decoder 621 and the memory array 611. The memory system 601 is a page 15 memory system with the memory cells 612 and 613 designated P1 to P32 and P33 to P64, respectively, and each of the memory cells 612 and 613 being operable to store a page.

To access the memory system 601 of the embedded control system 600 of FIG. 6, the processor 602 formats the address signals  $C_0 \dots C_M$  and  $C_M \dots (C_{M+N})$  to contain consecutive addresses associated with memory cells arranged along different rows of the 20 memory arrays 610 and 611. The row decoder 630, upon receiving and decoding the address signals  $C_0 \dots C_M$ , would activate row line RL1 to access memory cells P1, P9, P17, P25, P33, P41, P49 and P57; would activate row line RL2 to access memory cells P2, P10, P18, P26, P34, P42, P50 and P58; would activate row line RL3 to access memory cells P3, P11, P19, P27, P35, P43, P51 and P59; and would activate row line RL4 to access memory cells 25 P4, P12, P20, P28, P36, P44, P52 and P60. The row decoder 631, upon receiving and decoding the address signals  $C_0 \dots C_M$ , would activate row line RL5 to access memory cells P5, P13, P21, P29, P37, P45, P53 and P61; would activate row line RL6 to access memory cells P6, P14, P22, P30, P38, P46, P54 and P62; would activate row line RL7 to access memory cells P7, P15, P23, P31, P39, P47, P55 and P63; and would activate row line RL8 to 30 access memory cells P8, P16, P24, P32, P40, P48, P56 and P64. The column decoders 620 and 621, upon receiving and decoding the address signal  $C_M \dots (C_{M+N})$ , would operate in

association with the row decoders 630 and 631, respectively, by activating the respective column lines CL1 to CL8 accordingly. Pages from the accessed memory cells are output in the form of the data signal DATA [0:X]. Therefore, in a common data read or write scenario in which pages must be cyclically and sequentially read from, or written to, only a small 5 number of memory cells of the memory system 601, such as memory cells designated P1, P2, P3, P4, P5, P6, P7 and P8, the embedded control system 600 would effectively distribute read disturb stress across eight different rows of the memory arrays 610 and 611 (in combination) and across two memory blocks.

The addressable memory systems of FIGs. 2, 3, 5 and 6 may be burst mode memory 10 systems that minimize read disturb by initiating, responsive to a first memory address, a first burst access to access a plurality of bits from a storage element of a first row of a memory array, and initiating, responsive to a second memory address consecutive to the first memory address, a second burst access to access a plurality of bits from a storage element of a second row of the memory array. In the burst mode memory system, a single memory address is 15 used to access information from a series of sequential storage elements of a memory array.

During a burst mode read operation, it takes two clock cycles to access a page, and one clock cycle to read each word within the page. Further accessing of another page requires two more clock cycles regardless of whether the second page is located on the same row or different row as the previous page. A row line is ramped up and down on each clock cycle.

20 The ordering of the "PAGES WITHIN ROW" bits and the "ROWS WITHIN BLOCKS" bits of the addressing format 700 of FIG. 7 facilitate access of consecutively addressed pages on different rows of the memory array. While the burst mode memory system using the addressing format 700 of FIG. 7 and a conventional burst mode memory system using the conventional addressing format 900 of FIG. 9 both use the same amount of power and

25 number of clock cycles to access pages, only the burst mode memory system using the addressing format 700 of FIG. 7 will effectively spread read disturb across multiple rows of the memory array.

FIG. 8 illustrates, in schematic form, a portion of a memory array 800 for use in the memory systems 200, 301, 501 or 601 of FIGs. 2, 3, 5 or 6, respectively. The memory array

30 800 is made up of floating gate-type memory cells arranged in a plurality of rows and columns through interconnection by row lines RL1 and RL2 and column lines CL1 to CL4.

In particular, row line RL1 interconnects memory cells 850, 860, 870 and 880, each of which is representative of the memory cells of the memory array 800. Activation of particular combinations of row lines and column lines will access a memory cell for a read operation. The memory cell 880 comprises a control gate 810 that functions as the input of the memory cell, a floating gate 820, a source 840 and a drain 830 that functions as the output of the memory cell. The control gate 810 is connected to the row line RL2. The floating gate 820 stores charge indicative of the state of the memory cell. The drain 830 is connected to the column line CL1. The source 840 is connected to a common node via line SOURCE. In an embodiment where the memory cell 880 is a Flash EEPROM cell, the memory cell 880 is read by setting the row line RL1 to a voltage level of 2.5 V to 5 V, biasing the column line CL1 to a voltage level of 0.5 V to 1.5 V, and using a sense amplifier (not shown) to measure the current on the column line CL1 in order to determine whether the memory cell 880 is programmed or erased.

As an example of how read disturb affects a particular row of memory cells, consider the case where a read operation is to be performed on the memory cells 850, 860 and 870 in sequence. The row line RL2 is activated, and the column lines CL2, CL3 and CL4 are activated in sequence to read the information therefrom. Note that even though the memory cell 880 is not activated for reading, row line RL2 still holds a bias voltage on the control gate 810 of the memory cell 880 while reading information from the memory cells 850, 860 and 870. Thus, while no data is being read from the memory cell 880, reading data from the memory cells 850, 860 and 870 still contributes to a possible read disturb failure of the memory cell 880. In cases where a small program of instructions continuously accesses the same memory cells (e.g., the memory cells 850, 860 and 870) for a long period of time, the constant bias voltage maintained on the control gate of all memory cells connected to the same row line (e.g., row line RL2) can contribute to read disturb.

Many applications exist for the embodiments illustrated in FIGs. 2, 3, 5 and 6. Such embodiments may be readily employed in an embedded control system used in automotive applications. The processors 302, 502 and 602 may be microprocessors such as those used in wireless communication devices, and the memory arrays 310, 311, 510, 511, 610 and 611 may be used to store operating system instructions executable by the processor 302, 502 and 602. The memory systems 301, 501 and 601 may be formed on the same substrate and/or

included in the same package as the processors 302, 502 and 602, respectively. It will be appreciated that other processor and/or memory types and configurations may be implemented according to the principles set forth herein.

5 While the above is specifically described with respect to minimization of read disturb caused by read operations, it will be recognized that the memory systems 200, 301, 501 and 602 may minimize gate disturb that can occur during write operations. For example, gate disturb may be minimized in the case where the memory systems 200, 301, 501 and 602 employ EEPROM and consecutive EEPROM cells are repeatedly rewritten.

10 In the foregoing, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art will appreciate that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

15 What is claimed is: